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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/686,539	10/11/2000	Jeff Schulz	FORE-81	5750

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EXAMINER	
NG, CHRISTINE Y	
ART UNIT	**PAPER NUMBER**
2663	

DATE MAILED: 03/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No: 09/686,539	Applicant(s) SCHULZ, JEFF	
	Examiner Christine Ng	Art Unit 2663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 9* is/are rejected.

7)☒ Claim(s) *2-8 and 10-15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 October 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,878,039 to Gorshe et al in view of U.S. Patent No. 6,707,789 to Arslan et al.

Gorshe et al disclose in Figure 1 a switch of a network for switching data comprising a fabric (Elements 34, 36, 38, 40, 46 and 52) for switching the data and a parity fabric (Elements 30 and 32). The switch also contains a connection mechanism (Element 9) connected to the fabric (Elements 34, 36, 38, 40, 46 and 52) for providing data to and from the fabric (Elements 34, 36, 38, 40, 46 and 52) and connected to the parity fabric (Elements 30 and 32) for providing parity data to and from the parity fabric (Elements 30 and 32). Refer to Column 3, lines 21-28.

The switch comprises a first port card (Element 10) which receives data from the network. "Bytes of data flowing into the interface unit are input immediately into the input port data latches 30,32 which receive data through their respective input ports 10 and 12" (Column 7, lines 28-31). The first port card (Element 10) performs first parity calculations on the data received at the first port card (Element 10) and produces first parity data from the first parity calculations. The input port latch (Element 30) of the first

port card (Element 10) "contains a parity check circuit which provides indications at the Parity Error outputs that parity errors have occurred" (Column 7, lines 37-39). Refer to Column 7, lines 28-48. The first port card (Element 10) is connected to the connection mechanism (Element 9) to send data to the fabric (Element 34, 38 and 46) at the connection rate and to send the first parity data to the parity fabric (Element 30) at the connection rate. The input port accepts data at a first payload data rate and the output port outputs data at a second payload data rate. Refer to Column 6, lines 25-31. As shown in Figure 4, the input port receives data at 38.88 Mbps but can switch data rate to 19.44 Mbps as the data travels through the switch fabric.

The switch comprises a second port card (Element 12) which receives data from the network. "Bytes of data flowing into the interface unit are input immediately into the input port data latches 30,32 which receive data through their respective input ports 10 and 12" (Column 7, lines 28-31). The second port card (Element 12) performs second parity calculations on the data received at the second port card (Element 12) and produces second parity data from the second parity calculations. The input port latch (Element 32) of the second port card (Element 12) "contains a parity check circuit which provides indications at the Parity Error outputs that parity errors have occurred" (Column 7, lines 37-39). Refer to Column 7, lines 28-48. The second port card (Element 12) is connected to the connection mechanism (Element 9) to send data to the fabric (Elements 36, 40 and 52) at the connection rate and to send the second parity data to the parity fabric (Element 32) at the connection rate. The input port accepts data at a first payload data rate and the output port output data at a second payload

data rate. Refer to Column 6, lines 25-31. As shown in Figure 4, the input port receives data at 38.88 Mbps but can switch data rate to 19.44 Mbps as the data travels through the switch fabric. The second port card (Element 12) also separates the data into streams of data that together equal the data received at the second port card that are sent concurrently at the connection rate to the fabric (Elements 36, 40 and 52) and combines the data streams received at the connection rate into data that is sent to the network. The input port latch (Element 32) of the second input port (Element 12) handles "20 bits of data in parallel as a 10-bit high byte and a 10-bit low byte" (Column 7, lines 34-35). Data is outputted to the corresponding output port (Element 16) as a 9-bit high byte and a 9-bit low byte. Refer to Column 3, lines 16-21.

Gorshe et al do not disclose that the first input port card receives data at a first rate and the second input port card receives data at a second rate.

Arslan et al disclose in Figure 1 a SONET switch (Element 100) coupled to line interface units 104, 114 and 124. Each line interface unit 104, 114 and 124 has ports that can handle different OC-N data rates. Refer to Column 1, lines 23-39. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include that the first input port card receives data at a first rate and the second input port card receives data at a second rate; the motivation being so that the switch can support different rates since different telecommunication systems require different bit rates; thereby allowing the switch to accommodate more applications.

Allowable Subject Matter

3. Claims 2-8 and 10-15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

4. Applicant's arguments filed October 21, 2004 have been fully considered but they are not persuasive.

Referring to the argument that the same element was used as both a parity fabric and as a port card (page 8, lines 6-16), the input port card is element 10,12 and the parity fabric is the parity check circuit inside input port data latch 30,32. As stated in the office action (page 2, line 26 to page 3, line 2), "The input port latch (Element 30) of the first port card (Element 10) "contains a parity check circuit which provides indications at the Parity Error outputs that parity errors have occurred" (Column 7, lines 37-39)." Input port card 10, which is connected to input port data latch 30, forms an input port card that performs parity calculations on incoming data using the parity check circuit. Refer to Column 7, lines 28-46.

Referring to the argument that input port data latches 30,32 are distinct from the input port and that no parity calculation occurs at the input port (page 9, lines 9-14), refer to Column 7, lines 28-46. Data port latches 30,32 receive data through respective input ports 10,12 and are therefore connected to form an input port for data. The parity check circuit is also a separate element within data port latch 30,32 as shown by the dashed line in Figure 1A.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christine Ng whose telephone number is (571) 272-3124. The examiner can normally be reached on M-F; 8:00 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Ngo can be reached on (571) 272-3139. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

C. Ng CN
March 10, 2005

RICKY NGO
PRIMARY EXAMINER

3/14/05